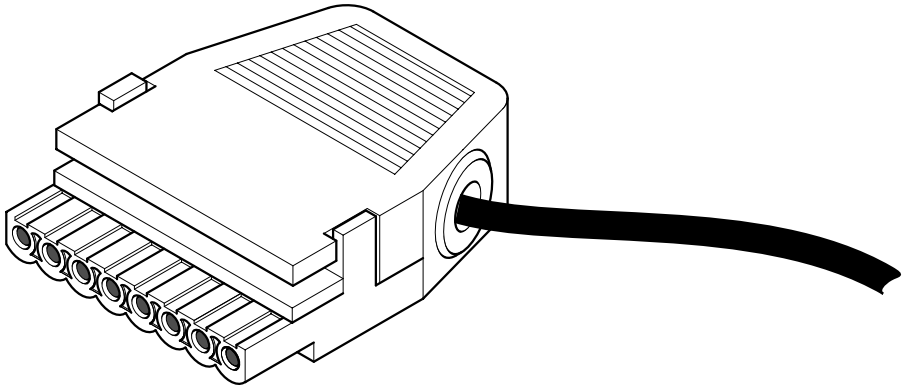
USER MANUAL

From February 1st, 2017 SAMES Technologies SAS becomes SAMES KREMLIN SAS
A partir du 1/02/17, SAMES Technologies SAS devient SAMES KREMLIN SAS

SAMES KREMLIN



SSI CONVERTER (Ang)

Type of amendment: Reworking the existing document

Written by:	Reviewed by:	Reviewed by:	Approved by:
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1. INTRODUCTION

1.1 PURPOSE OF THE DOCUMENT

This document contains the technical specifications for the product known as the SSI CONVERTER.

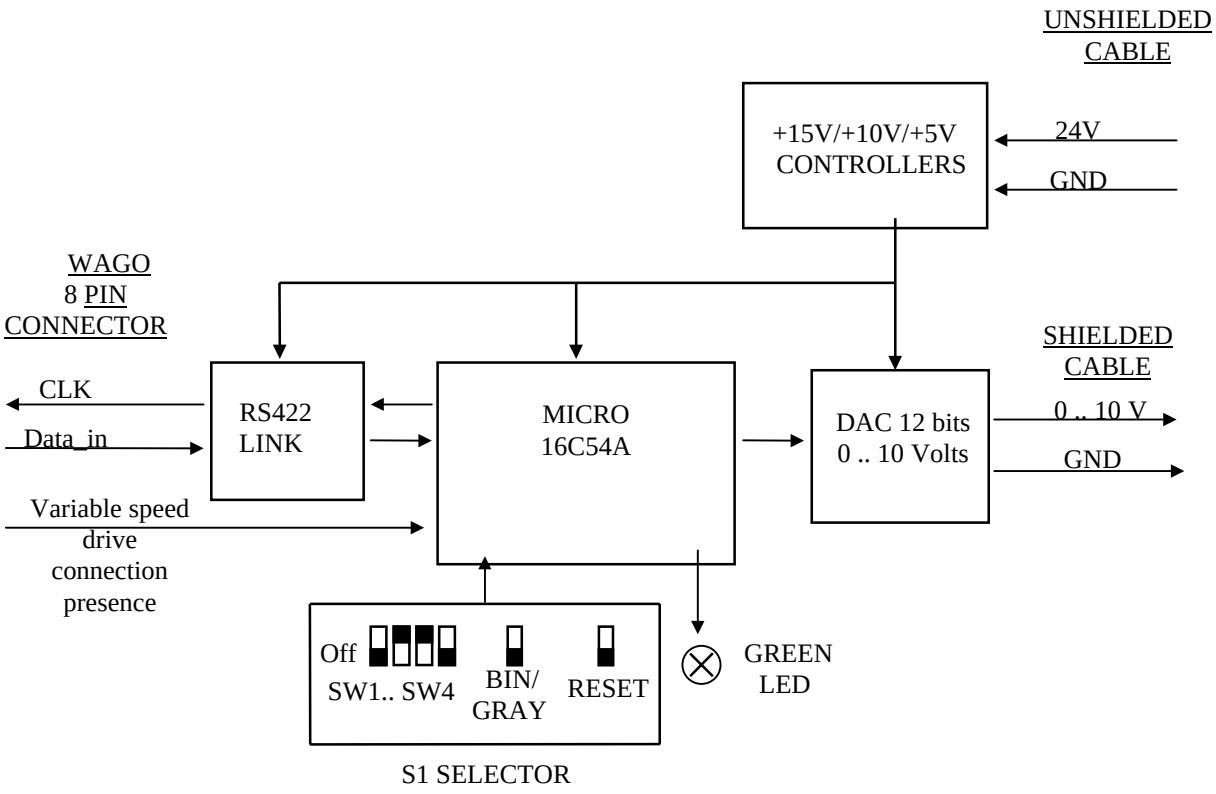
1.2 GENERAL DESCRIPTION

The SSI CONVERTER converts SSI coded information (representing a position coming from a multi-turn absolute coder) supplied by an ECODRIVE INDRAMAT variable speed drive, into an 0-10 Volt analog signal.

2. PRODUCT HARDWARE DESCRIPTION AND STRUCTURE

2.1 HARDWARE ARCHITECTURE

BOARD BLOCK DIAGRAM



2.2 MICROPROCESSOR SUPPLY

- External supply: 24Volts DC +/- 5%.
- Polarity reversal protection.
- Filtering: EMC.

Test: microbreak generation, slow power buildup, correct operation between 22 and 26VDC, non-destructive polarity reversal.

- Supplies: 5V +/-5%, 10V +/- 0.5%, 5V +/-5% .
- MICROCHIP OTP microcontroller: PIC16C54A.
- Digital to analog converter 12 bits, serial, +/- ½ LSB, 0-10V: LTC1257.
- RS422 interface.

Test: supply metering, generation of an SSI coded signal from an absolute coder in order to measure the 0-10V output.

2.3 INPUT/OUTPUT DEFINITION

- RS422 link:1 driver, 1 receiver
  Output voltage: Voh = 3.5V min.
  Vol = 0.4V max.
  Differential input threshold voltage: -0.2V min., 0.2V max.
  Max. frequency: 300Khz.
  Link length: 20 cms max.
- 0-10V output: Slew rate: 1V/µs min.
  Output impedance: 300 Ohms max.
  Offset error: +/- 8 LSB max.

2.4 CONNECTIONS

WAGO 8-pin socket connector without locking, on the variable speed drive side.
AWG22 gauge cables (0.34mm2), 2m long, on the 0-10V output side.

- 1 shielded signal cable:
  White wire = signal.
  Light blue wire = 0 Volts.
- 1 unshielded 24 volt supply cable:
  Red wire = 24 Volts.
  Black wire = 0 Volts.

The cables will be welded to the printed circuit, with no connector on the other end.

2.5 ENVIRONMENT

Operating temperature: 0°C to 50°C.
Storage temperature: -20°C to 70°C.
Relative humidity 25% to 75% without condensation.
Vibration 1 Gmax.

Test: oven checking of proper product operation from 0°C to +60°C .

2.6 MECHANICAL CONSTRAINTS

Enclosure dimensions: Length = 55mm max. (excluding connector).
Width = 43mm max.
Product protection index: IP21.
The LED will be visible on the face of the enclosure opposite that of the connector.
When the SSI Converter is connected to the variable speed drive, the cables should be routed downwards.
A label showing the configuration of the 5 switches (SW1 to SW4, BIN/GRAY) will be stuck on the outside of the enclosure, on one of the sides.

2.7 EMC QUALIFICATION TESTS

General Emission EN 50081-1:
Radiated emission EN 55022 class B.
Conducted emission EN 55022 class B.
General Immunity EN 50082-1:
Radiated immunity IEC 801-3.
Electrostatic discharges IEC 801-2.
Conducted immunity IEC 801-4.

2.8 OVEN DRYING TESTS

The enclosure is placed in an oven, and subjected to hot/cold cycles (0°C to 60°C).

Test: checking proper operation.

3. FUNCTIONAL SPECIFICATIONS

3.1 INTRODUCTION

An interface is produced, whose input is a value coded over 24 resolution bits derived from an ECODRIVE INDRAMAT Variable Speed Drive, and whose output is an analog voltage of between 0 and 10 Volts.

The switch (Bin/Gray) mounted on the board will enable BINARY or GRAY decoding of the 24 bits received, and must therefore be configured according to the type of sensor.

A value coded on 12 resolution bits will enable 0-10 Volts voltage supply. These bits will be obtained by means of a 12 bit window sliding over the 24 acquisition bits, where window position is defined by the 4 switches (SW1 ..SW4).

A binary input will inform the SSI CONVERTER of the status of the RESET switch and whether or not the Variable Speed Drive is connected.

A LED will indicate that the application is running properly by flashing at 1 Hz. Its status will be fixed if a fault occurs.

List of input items:

- Digital data over 24 synchronous serial bits (binary or gray).
- 4 binary inputs for position of the conversion window.
- 1 binary input to determine the type of coding received.
- 1 binary input validating connection to the Variable Speed Drive or status of the RESET switch.

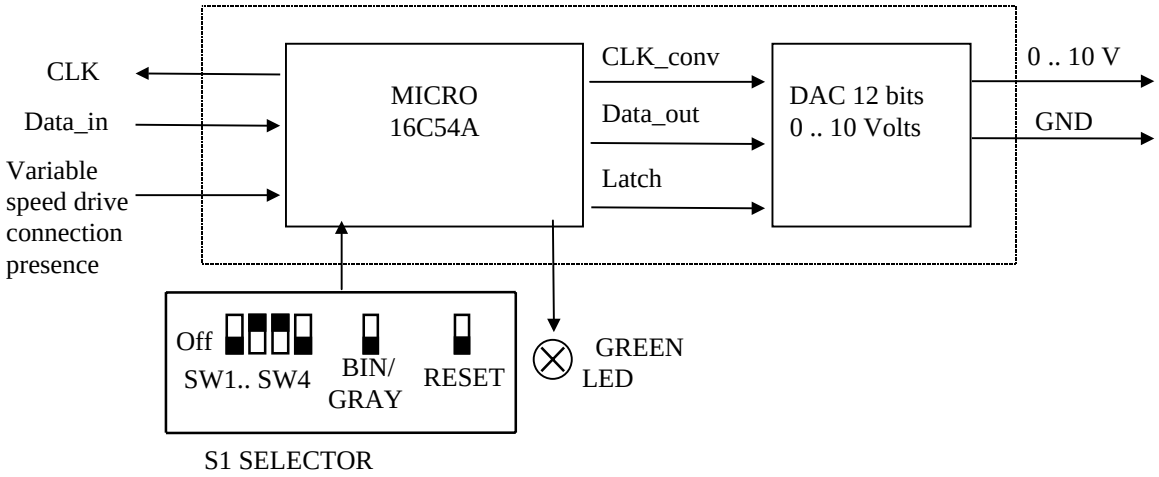
List of output items:

- A data acquisition clock signal.
- An 0-10V analog voltage with a 12 bit resolution.
- An activity LED.

The various constraints are:

- A digital data acquisition clock frequency of between 32Khz and 300KHz with a minimum synchronisation time of 100 µs.
- A stable update period.
- A reliable system (need for a software watchdog)

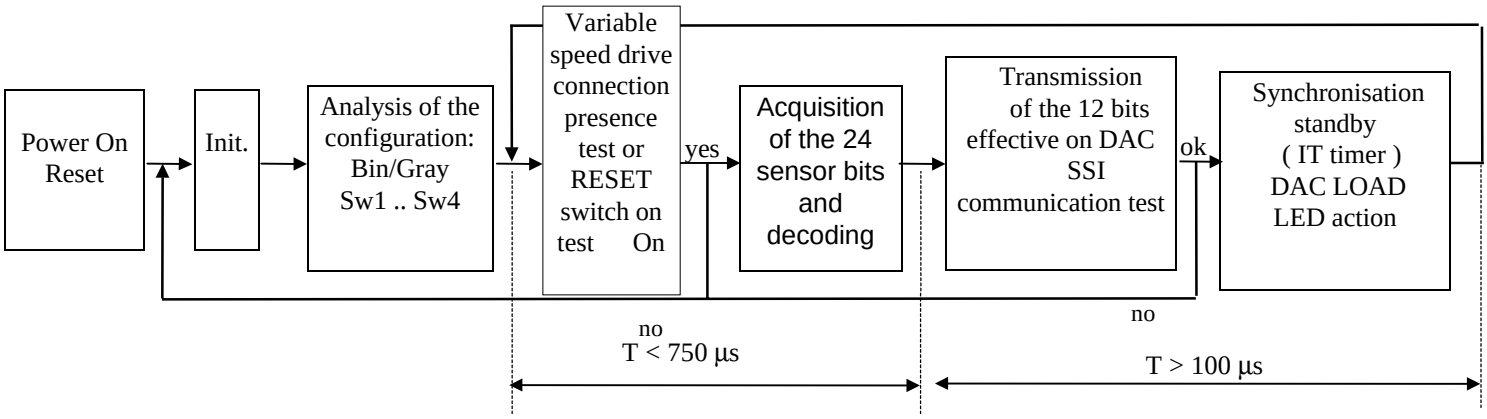
3.2 SOFTWARE GENERAL BLOCK DIAGRAM



The various switches will be taken into account each time the SSI CONVERTER is switched on, then each time the Variable Speed Drive is disconnected and the RESET switch is in the Off position.

To meet the various time constraints, the programme will be linear and a single interruption will ensure a fixed output voltage update period.

The programme sequence is shown below:



3.2.1 INITIALISATION

- Initialisation of the microprocessor and timer.
- Activation LED in the lit position.
- Transmission of 0 bits to the DAC in order to position the output at 0 Volts.

3.2.2 CONFIGURATION ANALYSIS

This phase in the programme analyses the switchs (SW1, SW2, SW3, SW4, BIN/GRAY).

The value supplied by SW1 .. SW4 will determine the 12 bits of the analog conversion (position of a 12 bit window on the 24 acquired bits), and the status of the activation LED.

CONFIG.	SW1	SW2	SW3	SW4	LED	Bits transmitted to the DAC
1	ON	ON	ON	ON	Flashes	bit 11 to bit 0
2	OFF	ON	ON	ON	Flashes	bit 12 to bit 1
4	ON	OFF	ON	ON	Flashes	bit 13 to bit 2
8	OFF	OFF	ON	ON	Flashes	bit 14 to bit 3
16	ON	ON	OFF	ON	Flashes	bit 15 to bit 4
32	OFF	ON	OFF	ON	Flashes	bit 16 to bit 5
64	ON	OFF	OFF	ON	Flashes	bit 17 to bit 6
128	OFF	OFF	OFF	ON	Flashes	bit 18 to bit 7
256	ON	ON	ON	OFF	Flashes	bit 19 to bit 8
512	OFF	ON	ON	OFF	Flashes	bit 20 to bit 9
1024	ON	OFF	ON	OFF	Flashes	bit 21 to bit 10
2048	OFF	OFF	ON	OFF	Flashes	bit 22 to bit 11
4096	ON	ON	OFF	OFF	Flashes	bit 23 to bit 12
1	OFF	ON	OFF	OFF	Lighted	bit 11 to bit 0
1	ON	OFF	OFF	OFF	Lighted	bit 11 to bit 0
1	OFF	OFF	OFF	OFF	Lighted	bit 11 to bit 0

The configuration of the BIN/GRAY switch will determine the decoding type

ON ===> GRAY.
OFF ===> BINARY .

3.2.3 VARIABLE SPEED DRIVE PRESENCE/ RESET SWITCH TEST

In order to validate configuration of switches SW1 to SW4 and BIN/GRAY and for the programme to move to the 24 bit acquisition phase, the Variable Speed Drive connection must be effective or the RESET switch (last switch on selector S1) must be on the ON position. Otherwise the programme will return to the initialisation phase.

3.2.4 ACQUISITION OF THE 24 BITS

The first 24 clock strokes enable acquisition of the 24 bits.
The data (n rank bit) is read on the falling edge of the CLK clock.
Bit 23 is the first bit acquired from each frame.
On the rising edge of the CLK clock, the bit is processed according to the position of the Bin/Gray switch then stored in the « DATA » register (3 bytes).
The data (PFB: power failure bit) read on the falling edge of the 25th clock stroke is not processed.
This routine hands over to the next routine at the 25th (and last) clock stroke, and leaves the CLK signal at « 1 ».

3.2.5 SSI COMMUNICATION TEST AND TRANSMISSION TO THE DAC

An SSI communication validity check is run, and the following observed:
- A piece of data at 0 read 5 microseconds after the rising edge of the 25th clock stroke.
- Then a piece of data at 1 read at the end of this routine, i.e. at least 30 microseconds after the rising edge of the 25th clock stroke.

Transmission of the 12 bits defined by the « CONFIGURATION ANALYSIS » routine to the digital to analog converter.
Transmission of the rank n bit on the falling edge of the CLK_conv clock.
The transmitted bit is entered by the converter on the rising edge of the CLK_conv clock.

If there is no SSI communication fault, this routine hands over to the next routine at the 12th clock stroke, and leaves the CLK-conv signal on « 1 ». Otherwise the programme returns to the initialisation phase.

3.2.6 SYNCHRONISATION STANDBY

This routine manages lighting of the activity LED according to the result of the « CONFIGURATION ANALYSIS » routine, then enters the IT TIMER standby mode.

When IT occurs, the LOAD signal is generated to the DAC, and the « SYNCHRONISATION STANDBY » routine hands over to the VARIABLE SPEED DRIVE PRESENCE TEST » routine.

3.2.7 WATCH DOG

This system security mechanism is designed to monitor proper running of the above-mentioned routines. It produces a software RESET in the event of a malfunction.